



Architectures for Computer Vision: From Algorithm to Chip with Verilog

Hong Jeong

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This book provides comprehensive coverage of 3D vision systems, from vision models and state-of-the-art algorithms to their hardware architectures for implementation on DSPs, FPGA and ASIC chips, and GPUs. It aims to fill the gaps between computer vision algorithms and real-time digital circuit implementations, especially with Verilog HDL design. The organization of this book is vision and hardware module directed, based on Verilog vision modules, 3D vision modules, parallel vision architectures, and Verilog designs for the stereo matching system with various parallel architectures.

- Provides Verilog vision simulators, tailored to the design and testing of general vision chips
- Bridges the differences between C/C++ and HDL to encompass both software realization and chip implementation; includes numerous examples that realize vision algorithms and general vision processing in HDL
- Unique in providing an organized and complete overview of how a real-time 3D vision system-on-chip can be designed
- Focuses on the digital VLSI aspects and implementation of digital signal processing tasks on hardware platforms such as ASICs and FPGAs for 3D vision systems, which have not been comprehensively covered in one single book
- Provides a timely view of the pervasive use of vision systems and the challenges of fusing information from different vision modules
- Accompanying website includes software and HDL code packages to enhance further learning and develop advanced systems
- A solution set and lecture slides are provided on the book's companion website

The book is aimed at graduate students and researchers in computer vision and embedded systems, as well as chip and FPGA designers. Senior undergraduate students specializing in VLSI design or computer vision will also find the book to be helpful in understanding advanced applications.

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